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Title*: *Photo Imager with Shared Reset FET and Pixel Amplifier

Continuing Application Data

This is a continuation in part of earlier co-pending patent application Ser. No. 09/768,124, which is a continuation in part of Application Ser. No. 09/490,374, filed Jaunaruy 24, 2000, now U.S. Pat. 6,590,198, July 8, 2003, which is a continuation in part of Application Ser. No. 09/039,835, filed March 16, 1998, now U.S. Pat. 6,084,229, July 4, 2000.

Background of the Invention

This invention concerns solid state imagers, and in particular is directed to an improved configuration of the pixels within a given column of a solid state imager. The invention is more particularly concerned with a pixel configuration that reduces the number of FETs associated with each given pixel so as to maximize the area available for collection of light.

Solid state image sensors are used in a wide variety of applications, and there has been much interest in pursuing low-cost, high-resolution, high-reliability image sensors for such applications. CMOS technology is well suited for imagers that are intended for portable applications, because of their need for a only a single power supply voltage, their ruggedness, and their inherent low power consumption. There has been great interest in achieving extremely high resolution also, which requires increased pixel density.

In imaging systems, there is a great desire for each pixel to have low noise, a high fill factor, and the smallest possible number of transistors per pixel, while maintaining quality and maximizing yield, i.e., imager chips per wafer. Pixels having only one transistor per pixel have been available only in passive imager designs, which have an inherent high noise threshold. Passive pixel designs are pixels that do not buffer the photon-generated charge during read out, with the result that there is either high noise, such as with photodiodes and charge-injection devices (CIDs) or else the information is destroyed during read out, as in charge-coupled devices (CCDs). The single FET per pixel is thus used only for addressing during reading, and not for buffering.

Imager designs that employ pixels that buffer their signal prior to read out are known,

such as active pixel sensors (APSs) and active column sensors (ACSs). These designs typically have three FETs per pixel, and achieve a much lower thermal noise than seen in passive pixel designs. However, because much of the available surface area of each pixel is occupied by these transistors, and by various power and control wires that have to cross the pixels, there is less area available for the active photosensor elements.

The ideal imager will have its pixels designed to have low noise, a high fill factor, require few or no transistors, a 100% manufacturing yield, and close to zero unit cost.

Active pixel sensors, or APS sensors suffer from fixed-pattern noise or FPN and typically require three or more transistors per pixel. Numerous APS designs have added many extra FETs to overcome FPN, with some designs having as many as thirty-seven FETs per pixel (S. Kleinfleder, S. Lim, X. Liw and A. El Gamal, "A 10000 Frames/S CMOS Digital Pixel Sensor," IEEE Journal of Solid State Circuits, Vol. 36, No. 12, December 2001). However, adding more transistors to each pixel reduces the fill factor and increases the unit cost for the imager.

ACS imagers enjoy very low fixed pattern noise, but still require at least two FETs, and normally three to four FETs per pixel, and reducing the number of FET's below this requirement will increase manufacturing yield as well as improve fill factor. An active column sensor (ACS) architecture has recently been developed, as disclosed in Pace et al. U.S. Pat. No. 6,084,229, which permits a CMOS image sensor to be constructed as a single-chip video camera with a performance equal to or better than that which may be achieved by CCD or CID imagers.

As mentioned above, APS and ACS sensors have three to four FETs for each pixel. As APS sensors suffer from FPN, many designs have added extra FETs to minimize this source of noise and distortion. Also pixel complexity has increased in many designs in order to provide additional pixel functions, such as shuttering capabilities for exposure control. However, even with only three FETs per pixel, a 1.3 mega-pixel imager will require 3.9 million transistors for the pixel array alone. The three transistor limit how small each pixel can be for a given set of process rules. Once most of the pixel area has been consumed by transistors, there is little room left to collect light, and so the conventional approach is to add micro-lenses to the imager to increase the fill factor optically. While micro-lenses permit smaller pixel size for a given set of

process rules, the micro-lenses add cost to the wafer processing, and require yet another process step that can generate defects and reduce wafer yield. Therefore, the micro-lens approach is less attractive than an alternative that would increase the area of each pixel that is available for collecting light. Also, using fewer transistors per pixel would permit a number of design options, such as maintaining the pixel size and avoiding the need for micro-lenses, or increasing the pixel density by making the pixel size smaller and adding micro-lenses, or else following older and lower cost design rules for the same size pixel and also adding micro-lenses.

In order to obtain the lowest cost for a solid-state sensor, where cost is based on size or total area, it has been a goal to produce an imager which achieves the smallest size possible for an equivalent number of pixels. Typically, this would require reducing pixel size or size of the photosensitive areas down to the design limits of the process. This is especially important if the same chip has to devote a significant amount of area for its various output multiplexers and output amplifiers. Ideally, size reduction should be achieved, not by reducing the pixel photosensitive areas, but rather by reducing the area consumed by the other circuitry which is located within the pixels.

By combining the ACS technology of U.S. Pat. No. 6,084,229 and an improved pixel structure of U.S. Pat. No. 6,232,589, that is, a so-called Charge Snare Device or CSD, a pixel can designed that needs only two FETs per pixel. One of the two FETs is a sense FET, or pixel output transistor, that forms a part of the pixel column amplifier, and the other FET is a reset FET, which is needed to reset the sense node at the gate of the sense FET. In the CSD pixel arrangement, two of the usual FETs found in the prior photo-gate design, namely, the transfer FET and the select FET, are eliminated.

In the CSD-based imager of U.S. Pat. No. 6,232,589, the pixels operate without a separate selection gate. First the sense node, i.e., the input to the pixel output amplifier FET, is set to ground by gating the reset FET (which is an N-FET), so that the sense node FET is biased off and therefore isolated from the rest of the shared FETs in the same column. Thereafter, addressing of the sense FET is carried out by resetting the sense node FET from ground to 2.5 volts (for a 3.3 volt process). The photon-generated charge is collected by the photogate when a

bias is applied and the active region of the silicon has been depleted. After the desired integration time, the sense node FET is selected by setting it to 2.5 volts, as just discussed. The collected photon-generated charge is transferred to the sense node when the bias applied to the photogate is removed, e.g., to 0.0 volts. The sense node, which is tied to the gate of the sense FET, physically surrounds the photogate, either completely or nearly so. The sense node connects with the gate of the sense node FET and the drain of the reset FET, as well as the sense gate of the CSD. The collected photon generated charge drifts and diffuses to the sense node. The sense node captures all or nearly all the collected charge at the photogate, as the photon-generated charge is surrounded or "snared." This technique of sensing photon-generated charge has very low noise, as the thermal noise on the sense node can be removed by first sampling the sense node just after reset to measure background that contains such noise, and then remeasuring the sense node after the photon-generated charge has been transferred, and taking the difference between these two measurements as a pixel output. The thermal noise that is generated is correlated and subtracted, that is, the device carries out true correlated double sampling or CDS.

It would be desirable to use the same general concepts to create an imager in which the pixels had only a single FET associated with the photogate thereof, and which had the advantages of low noise and true CDS, but a single-FET design has eluded those working in this art.

Objects and Summary of the Invention

Accordingly, it is an object of the present invention to provide a solid-state imager that avoids the drawbacks of the prior art.

It is another object to provide an imager that increases the amount of each pixel that is occupied by its photosensitive portion, without encountering other problems, such as fixed pattern noise.

It is another object to simplify the pixel structure of the solid state imager.

Likewise, it is an object to provide a solid-state imager that achieves a reduction in the number of FETs required, i.e., requiring on average a single FET per pixel.

In accordance with one aspect of the present invention, a solid-state area or linear imager is made as an array of pixel elements extending in columns and rows. The objective of reducing

the number of FET's per pixel is achieved by sharing the reset and sense node FETs between two or more photo sensitive regions, i.e., between two or more pixels. This is possible because the sense node is idle for the overwhelming majority of the time, during which frame integration takes place, and the sense node is only actuated for a very brief interval just after a given row is reset for selection and reading of the pixel information. The pixel (e.g., charge snare device) that has a gate signal applied to it is the pixel that has its photon-generated charge transferred to the sense node. The sense node can be a photogate as discussed, or may alternatively be a reverse-biased diode, as the signal timing is the same for either.

According to any of a number of embodiments of the invention, the photosensitive array is comprised of a plurality of pixels arranged in columns and rows, wherein the pixels are configured into groups of at least a first pixel and a second pixel. There may be two or more than two pixels in the group sharing the FETs. A shared pixel output transistor, i.e., the sense FET, has a sense electrode and an output electrode, and a shared reset transistor has a gate coupled to receive a reset signal and an output, i.e., drain, coupled to the sense electrode of the associated shared pixel output transistor. Each of the first and second pixels has a photosensitive element with an output electrode coupled to the sense electrode of the shared pixel output transistor, and a gating electrode coupled to receive a respective first and second pixel gating signal.

The pixels of the group that share a common FETs can be in successive rows in the same column, or can be in adjacent columns in the same row. The group of pixels can comprise four pixels sharing a single output FET, or four pixels with two sharing one output FET and one reset FET and the other two sharing a second output FET and a second reset FET. By controlling the timing of the gate and reset signal, it is possible to "bin" or combine the photon-generated charge from the two pixels. Binning is useful for increasing sensitivity in low-light level environments. The imager can be configured as monochromatic or polychromatic (i.e., color), and the shared FET architecture of this invention can be used to great advantage where a Bayer pattern of color pixels is employed.

The solid-state imager of this advantage has the advantages of fewer FETs and fewer metallized strips or wires to carry signal and power to the pixels. This leaves more pixel area

available for light collection, and also results in a significantly lower manufacturing scrap rate, i.e., higher manufacturing yield and reduced manufacturing costs.

The above and many other objects, features, and advantages of this invention will be more fully appreciated from the ensuing description of a preferred and exemplary embodiment, which is to be read in conjunction with the accompanying Drawing.

Brief Description of the Drawing

Fig. 1 is a schematic diagram of an active pixel sensor configuration of the prior art.

Fig. 2 is a schematic diagram of an active column sensor configuration of the prior art.

Fig. 3 is a schematic diagram of a two-transistor charge snare device (CSD) of the prior art.

Fig. 4 is a schematic diagram of a pair of pixels that share a common ACS amplifier transistor and reset FET, according to one possible embodiment of this invention.

Fig. 5 is a schematic diagram of another embodiment of this invention.

Fig. 6 is a schematic diagram of another embodiment.

Fig. 7A to Fig. 7E are timing charts for explaining the operation of the FET per pixel sensors of the embodiments of this invention.

Fig. 8 is a diagram of a pixel layout of an embodiment of this invention.

Figs. 9 and 10 illustrates further embodiments of the invention, employing transfer gate technology.

Fig. 11 illustrates an embodiment employing transfer gates and color binning.

Detailed Description of the Preferred Embodiment

With reference now to the Drawing, and initially to Fig. 1 thereof, a CMOS imager 10, of the type that is known as an Active Pixel Sensor or APS, is shown here with a rather large number of components, including a photogate 12 which is the light sensitive member, with a transfer FET 12a, a row select transistor 14, a reset transistor 16, a sense FET 18, and various metallized leads including the row select lead SELECT, photogate lead PG, transfer lead TX, reset lead RESET, input drain voltage VDD, and output column bus COL BUS, which is connected to an output load. The APS imagers tend to have at least three and often many more

FETs for each pixel, with pixel complexity increasing in many designs due to the addition of other pixel functions such as shuttering capabilities for exposure control. Even with only three FETs per pixel, a 1.3 megapixel imager will have 3.9 million transistors in the pixel array alone. The three transistors are a lower limit of complexity in the APS system, and limit how small a pixel can be for a given set of process rules. Once most of the pixel area has been consumed by the transistors, there is little area left for collecting light. In many cases, microlenses are added to increase the light collection or optical fill factor, by concentrating the light into one portion of each pixel. However, this technique does add to the complexity, and hence cost, of the imager, and adds another step that can generate defects and hence reduce wafer yield. Therefore, it would be preferable, if possible, to employ fewer transistors and increase the photosensitive area of each pixel, or else (using microlenses) to reduce pixel size even further. By reducing the number of transistors per pixel, it would also be possible to reduce processing costs and increase reliability and yield, even if the pixel size is unchanged.

Active Column Sensor technology has been described earlier, e.g., in Pace et al. U.S. Pat. No. 6,084,229, which is incorporated herein by reference. Active Column Sensor (ACS) architecture can be applied to either a linear array or to a two-dimensional array. An illustration of an ACS imager is shown here in Fig. 2. As explained in U.S. Pat. No. 6,084,229, each pixel has a photodiode 22, and a pair of FETs in series, that is, a sense FET 24 and a select FET 26 incorporated into it, with the source electrode of the sense FET 24 and the drain electrode of the select FET 26 being connected by means of a pair of vertical conductors to respective inputs of an associated column amplifier circuit 28. A reset FET 27 has its drain connected with the gate of the sense FET 24. In the ACS sensor, the column amplifier is configured as a closed-loop unity gain amplifier (UGA), thereby ensuring gain and offset uniformity among all pixels of the respective column.. The column amplifier 28 is followed by a correlated double sampling (CDS) circuit 30 that corrects for offset voltages while providing a differential output voltage. The outputs of the various column amplifiers are supplied to respective inputs of a multiplexer circuit (not shown) that combines the output levels of the pixels of each selected row, in turn, and this combined output is then fed through a video output amplifier to provide an output video signal.

SELECT and RESET signals and Reset Bias are supplied to each row of pixels, in turn, so that the pixel FETs of the selected row connect to the column amplifier 28. This technology has the useful advantages over the prior APS technology of a smaller FET count per pixel, and a capability of cancelling out fixed pattern noise.

Fig. 3 illustrates the general construction of an imager 32 in the form of a charge snare device as described in Pace et al. U.S. Pat. No. 6,232,589, which is also incorporated herein by reference. In the CSD imager 32 each pixel 34 has a two-FET construction in addition to a sense gate 36. Here a photogate 38 is supplied with a photogate signal PG, and a sense node of the sense gate 36 is coupled to the gate of a sense FET 40. A reset FET 42 has a drain connected to a supply of Reset Bias, a source connected to the sense node, and a gate connected to receive a reset signal RESET. The source and drain electrodes of the sense FET 40 are connected to a column amplifier in the manner as shown in Fig. 2. The CSD architecture results in a two-FET pixel, as a separate selection gate can be avoided. The reset FET 44 is needed to restore the sense node and the gate level of the FET 42. The transfer FET and the row select FET are eliminated.

The operation of the CSD imager is straightforward. The sense node is set to ground (reset bias) by actuating the reset FET 42 (in this example, the reset FET 42 is an N-FET). Then the sense node is biased off, and is therefore isolated from the rest of the shared FETs in the column. Thus, addressing of the sense FET 40 in this example is carried out by resetting the sense node from ground to 2.5 volts (for a 3.3 volt process). The photon-generated charge is collected by the photogate 38 when a bias is applied and the active region of the silicon (shown in dash lines) has been depleted. After the desired integration time, the sense node is selected by resetting it to 2.5 volts via the reset FET 42. The collected photon-generated charge is transferred to the sense node, i.e., to the gate of the sense FET 40, when the reset transistor is gated off and the bias applied to the photogate 38 is removed. As explained in the U.S. Pat. 6,232,589, the sense gate 36 of the pixel image area at least substantially surrounds the photogate 38, and preferably completely surrounds the photogate 38. In this architecture, the sense node is comprised of the sense gate 36, the gate electrode of the sense FET 40 and the drain of the Reset FET 42. The collected photon-generated charge drifts and diffuses to the sense node, which

captures all or nearly all the collected charge of the photogate 38, such that the photon-generated charge of the photogate is surrounded or "snared." This technique of sensing the photon-generated charge has very low noise, as the thermal noise or KTC noise on the sense node can be removed by first sampling the sense node just after reset (to measure the background that contains KTC noise) and then re-measuring the sense node level after the photon-generated charge has been transferred to it, and employing the difference of the two levels as an output. The KTC noise that is present is correlated and is subtracted out for true Correlated Double Sampling or CDS.

An arrangement that reduces the number of FETs per pixel is shown in Fig. 4, in which the sense or output FET and the Reset FET are shared between two (or more) pixels of a column, or in the same row in adjacent columns. Here, a pair 50 of pixels includes a first pixel device 52 formed as a charge snare device with a photogate 53 and a sense gate 54, and a second pixel device 56 also with a photogate 57 and a sense gate 58. The sense gates 54, 58 form a part of the sense node together with a gate electrode of an output or sense FET 60 that is common to both pixel devices 52 and 56. A common reset bias FET 62 has its source connected to the sense node, and has drain and gate terminals connected to a supply of reset bias and to a line that supplies a RESET signal, respectively. The photosensitive regions or pixel devices can be composed of either photodiodes of photogates. The sense node is available for sharing between the two pixel devices 52 and 56 because the sense node is idle for the overwhelming majority of the time during frame integration and is only utilized for a small period of time just after a row is reset for selection and reading of the pixel information. Timing for a sense node that is either a reverse biased diode or a photogate is the same. Each pixel device accumulates photon-generated charge and each has its charge transferred to the sense node only at the time that the pixel device is to be read.

A simple form of the embodiments of this invention can be implemented with the two pixel devices of each pair located in successive rows in the same column. Actually, if the sense node is common between any two pixels in the same column, the operation would be the same. The readout of each pixel occurs by first resetting the sense FET 60 to the reset value, e.g., 2.5

volts, by actuating the reset FET 62. The readout of the photogate 53 comes by application of a gating signal PG1, and readout of the pixel value is accomplished by removing the bias from the photogate 53, e.g., going from 2.5 volts down to 0.0 volts, after the desired integration time. To read out the pixel value of the other pixel device 56, the process is repeated, but using a gating signal PG2 for controlling the photogate 57. This technique has a benefit of allowing true summation of pixels that are common to the same sense node, that is, a process commonly referred to a "binning." Binning is accomplished by transferring the photon generated charge onto the sense node from both pixel devices 52 and 56 at the same time, after the sense node FET 60 has been reset.

The embodiments such as the one described in connection with Fig. 4 have an architecture of two FETs for each pair of pixel devices, i.e., one FET per pixel, as the two FETs are shared between two pixels.

Fig. 5 illustrates an embodiment in which two pixels in the same row (and in adjacent columns) can share the same pixel amplifier FET 60 and the same reset FET 62, and share the same sense node. Here, the shared sense node along a common row is associated with a pair of photogate elements 70 and 72, with nodes controlled by photogate signals PG1 and PG2. The timing of signals is the same as described above in connection with the embodiment of Fig. 4. Here, there is a common conductive element 74 surrounding each of the photogates 76 and 78 of the respective pixels and defining the sense gate for both pixels. Photogates 76 and 78 for both pixels are isolated from the sense node in this illustration using field oxidation; any processing method of isolation including shallow trench, implants, and physical distance can provide the necessary separation between the sense node and photogates. The photogates herein are of polysilicon construction; but can also be a pinned photodiode, or any optical gate construction including an implanted virtual gate often used in CCDs, including the HyperHAD construction offered by Sory Corporation. This element 74 and the gate of the FET 60 define the sense node. In this embodiment, the element 74 can be formed of an N+ or N- region, with an optional P+ surface implant to minimize surface defects and the resulting dark current, and a metallization can be used for the photogates 76 and 78. An alternative arrangement is illustrated in Fig. 6,

wherein, in place of the element 74, a well 80 of N+ or N- material is used. Other elements shown in Fig. 6 can be identical with what is shown in respect to Fig. 5.

Figs. 7A to 7E show the signal timing sequence for reading out the optical signal from any of the three embodiments described just above. Initially, at the commencement of a readout sequence, the Reset Bias level goes from low to high (Fig. 7D), and permits sampling of background readout values. For the first of the two pixel elements of the pair, i.e., 52 or 70, the reset gating pulse RESET (Fig. 7C) samples the background value (**a** in Fig. 7E) by removing bias on the element 54 or 74, and then the photogate signal PG1 (Fig. 7A) is applied to photogate 53 or 76. This transfers the photon-generated charge onto the common sense node, and provides an output level (**b** in Fig. 7E). The process is repeated for the second pixel 56 or 72, except using the second pixel photogate signal PG2 (Fig. 7B), producing a respective second background value a and readout output level b as shown in Fig. 7E. The difference values **c1** and **c2** represent output pixel values that are corrected by means of true correlated double sampling. After readout, a new integration period begins, and other pixels in the array are sampled.

Fig. 8 illustrates, in very general terms, a possible layout for the pixels 52, 56 of the embodiment of Fig. 4, with vertical conductors 80 and 82 constituting a column bus, and horizontal conductors formed to include reset R1 and photogate signal conductors PG1 and PG2. The photosensitive areas are surrounded respectively by a pair of closed-geometry conductors as the sense gates 54 and 58, with one section being common to both sense gates to unify the same. The reset FET 62 and the pixel sense FET 60 are situated here above the two pixels 52 and 56. The sense gates 54, 58 completely surround the respective photogates 53, 57. In other possible embodiments, the sense gate substantially surround, or encompass a majority of the pixel photosensitive area, so as to capture all or nearly all of the photon-generated charge. A reverse-based diode can be used, composed as an N-type well in a P-type substrate. Other reverse biased diodes can be constructed, depending on the actual CMOS semiconductor process used to fabricate the pixels, so long as the sense nodes completely or nearly completely surround the photogates, so as to maximize charge-transfer efficiency or CTE. Ideally, the CTE should be at 100% or nearly 100%; however, in some applications, a known lower CTE can be employed to

extend the dynamic range of the sensor.

In the embodiments in which one amplifier and one reset FET are shared between two columns, the layout would be configured in a similar fashion, but with the two pixels arranged side by side in the same row. The arrangement of the pixel amplifier is described in U.S. Pat. 6,084,226 and the layout of the pixels using CSD architecture is described in U.S. Pat. 6,232,589.

Transfer-gate based pixel technology can be used in the pixel arrays according to this invention, and an example is shown here in Fig. 9. In Fig. 9, elements that are shared in common with the schematic of the embodiment of Fig. 4 are identified with similar reference numbers. Here, instead of CSD pixel devices, a first pixel is formed of a photogate device 153 and a transfer gate FET 154 connecting the same to a common sense node, with the second pixel also being formed of a photogate device 157 and a transfer gate FET 158. In this embodiment, additional conductors are provided in each row to bring transfer signals TX1 and TX2 to the transfer gate FETs 154 and 158. The pixel sense FET 60 and reset FET 62 are shared with both pixels, as in the previous embodiment. The readout sequence is also similar to those of the previous embodiments, providing true correlated double sampling or CSD.

An embodiment of this invention in which the sense FET 60 and the reset FET 62 are shared by a larger number of pixels is illustrated in Fig. 10. Here, there are four pixels 91, 92, 93, and 94, in each of two rows in two adjacent columns. The pixels here are formed using transfer gates, as in Fig. 9. However, other technology, such as CSD technology, could be used. Signal conductors are provided to transfer signals TX1, TX2, TX3, and TX4 and for photogate signals PG1, PG2, PG3, and PG4. The four transfer gates of these pixels all feed into a common sense node 95 that is connected with the gate of the pixel sense FET 60 and the drain of the reset FET 62. The four pixel arrangement as shown here can facilitate binning by reading out two of the pixels at the same time, or by reading out all four. True additive binning can be used for higher speed data transfer or for increased sensitivity. Binning can be carried out on the column axis or the row axis, or diagonally. All four photogates can be replaced by photodiodes (not shown) and the elimination of the four PG control signals. The operation of the photodiodes is similar except resetting the photodiodes to begin integration. Biasing of the photodiodes is by

resetting the sense node to the desired starting level of the photodiode and allowing the transfer signals to be ON (e.g., VDD) to bias the photodiode accordingly. Integration for photodiodes begins when thee reset FET is turned OFF (e.g., 0.0 Volts) and the corresponding transfer signal (TXn) is also turned OFF. Binning with photodiodes is not possible as the charge in the sense nodes will instead average with photodiode charge.

Fig. 11 illustrates an embodiment of this invention in which shared sense nodes are used for a color sensor. Here there are arranged on one column a first sense FET 60 and second sense FET 160, with associated reset FETs 62 and 162. Red, green, and blue filters are used, and the pixels are arranged into a Bayer pattern of Green1/Red/Green2/Blue in a two X two matrix. Here, green pixels 101, 102, 103 and 104 share the FETs 60 and 62. If a given application requires a lower resolution image but a higher frame rate or higher sensitivity, the true additive binning of the same color pixels can be easily carried out. This contrasts with the current technology which simply skips over unwanted pixels when it is desired to minimize the amount of data transferred, and which has an additional disadvantage in terms of reduced sensitivity. In this invention, all pixels can be sampled, keeping sensitivity high. Because binning can be carried out here at the level of the pair (or quad) of pixels, there is less need for processing on the periphery of the video imager or for off-chip processing. If all four pixels are binned together for a monochrome image, that would allow low-light-level image acquisition with only one CDS sample per four pixels binned together. The true CDS and the summation (binning) of four pixels allows for very low noise and high dynamic range. Filters can be applied in the same manner to Fig. 10, although that is not shown. Also, different filter configurations can be utilized and the shared sense node can be altered to match filter configuration.

The principle of sharing an output FET and a reset FET, to eliminate the select and/or transfer FET among one or more pixels could be applied to active pixel sensor (APS) imagers, utilizing a source follower configuration and photodiode pixels as well. Another advantage of using a shared node among a two-by-two matrix of pixels is the reduction of the number of distributed amplifiers from one per column to one per two columns, as shown in Fig. 11, with higher reductions possible. With pixel geometries going smaller and smaller it is becoming

difficult to place the analog and digital processing circuitry on the same pitch as the pixel. Since the processing circuits are repeated on a column by column basis, if the circuits only have to be repeated every other column, or less frequently, the repeat pitch is doubled for Fig. 11, and higher multipliers are possible if there are more pixels that share the same sense and reset FETs. Previously, the only alternative to the repeat pitch of the processing circuits was to alternate the column electronics, so that even columns had their electronics at the top of the pixel array, and the odd columns had the electronics brought to the bottom of the array (or vice versa). This would in effect break the imager into different sections, as indicated on Pat. No. 6,590,198 to Zarnowski et al, and as shown in Fig. 5. The video is effectively broken into different sections that are either brought out to different ports (or to different pins on the same package) or can be multiplexed back together. By utilizing this previously described method in addition to the technique of this invention, the repeat pitch can be doubled again, further facilitating the imager designer.

While the invention has been described with reference to specific preferred embodiments, the invention is certainly not limited to those precise embodiments. Rather, many modifications and variations will become apparent to persons of skill in the art without departure from the scope and spirit of this invention, as defined in the appended claims.